Low-noise fractional-N frequency synthesizer using reference multiplication and high-resolution time-to-digital converter using time-domain arithmetic circuits

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地點： 國立台灣大學電機二館124室

大綱： In the first part of the talk, techniques to achieve low-noise low-power fractional-N frequency synthesizer will be presented. In order to reduce quantization noise of delta-sigma modulator (DSM), reference multiplication technique is employed by means of nested and cascaded-PLL architecture. In the nested PLL, intermediate output of the feedback divider is used to clock the DSM at nine times the reference frequency and a band pass filter, implemented using a PLL, is added to suppress noise-folding. In a cacaded-PLL, reference injection is used for a integer-N bang-bang PLL that generates 16x reference clock for the following fractional-N PLL. In the second part of the talk, high-resolution high-speed time-to-digital converters (TDCs) will be described. By using time-domain arithmetic circuits such as time-adder, time-amplifier, and time-register, different types of energy-efficient TDCs are implemented such as two-step, pipelined and high-order oversampled TDCs. Prototype results in 65nm will be shown.

主講人簡介：

SeongHwan Cho received the B.S. degree in EE from KAIST, Korea, and the S.M. and Ph.D. degrees in EECS from MIT, Cambridge, MA, in 1997 and 2002, respectively. In 2002, he joined Engim, Inc., where he was involved in data converters and phased-locked loop (PLL) design for IEEE 802.11abg WLANs. Since November of 2004, he has been with KAIST in the department of EE, where he is now an associate professor. His research interests include analog and mixed-signal circuits for low power communication systems, bio/health-care devices and CMOS sensors. Prof. Cho was the co-recipient of the 2009 IEEE Transactions on Circuits and System Society Guillemin-Cauer Best Paper Award and 2012 ISSCC Takuo Sugano Award for Outstanding Far-East Paper. Prof. Cho serves on the Technical Program Committee on several IEEE conferences, including ISSCC, Symp. on VLSI and A-SSCC. He serves as associate editor of IEEE Trans. on Circuits and Systems-I from 2010 to 2011 and have served as guest editor of JSSC. He has twice received Outstanding Lecturer Award from the department of EE and KAIST.

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